Please cancel claims 1-5.

IN THE CLAIMS

1. (Cancelled) A meta-addressing architecture for a network of dynamically reprogrammable processing machines, the meta-address specifying a local memory destination for a data packet comprising:

a plurality of addressing machines, each addressing machine having a unique geographic address, for servicing interrupts, generating and transmitting meta-addresses comprising of a geographic address and a local address, and queuing messages;

a plurality of dynamically reprogrammable processing machines (DRPMs), each dynamically reprogrammable processing machine coupled to at least one addressing machine, for storing, retrieving, and processing data from a local memory unit responsive to received local-addresses;

a plurality of memory units, each memory unit associated with a DRPM; and

an interconnect unit, coupled to the addressing machines, for routing data between addressing machines responsive to the geographic address of the meta-address.

2. (Cancelled) The addressing machine of claim 1, wherein at least one of the addressing machines further comprising:

an address decoder, for decoding a received meta-address into a geographic address and a local address;

a control unit, coupled to the DRPM, local memory, and the address decoder, for retrieving meta-address information from the local memory responsive to receiving an imperative from the DRPM, assembling a data packet responsive to the retrieved meta-address, receiving geographic and local addresses from the address decoder, and transmitting a data packet to the DRPM responsive to determining a decoded geographic address matches an associated geographic address.

3. (Cancelled) The architecture of claim 1 further comprising:

a plurality of architecture description memory units, each one coupled to a DRPM, for storing a geographic address for the DRPM to which it is coupled.

4. (Cancelled) The apparatus of claim 2 wherein the addressing machine further comprises:

an interrupt handler, coupled to the I/O unit, comprising:

a recognition unit, for identifying interrupt requests;

a comparator, for comparing identified interrupt requests to a stored list of interrupt requests to verify validity of an interrupt request; and

interrupt logic, for processing a validated interrupt request in accordance with stored interrupt handling instructions.

5. (Cancelled) The meta-addressing architecture of claim 1 wherein the meta-address is 80 bits side, the geographic address is 16 bits wide, and the local address is 64 bits wide.

6. A method for processing instructions in a parallel processor architecture having local processing machines coupled to local addressing machines and local memory, and the addressing machines are identified by unique geographic identifications and are interconnected through an interconnection unit, comprising the steps of:

receiving a program instruction

determining if the received program instruction requires a remote operation;

responsive to a remote operation being required, storing remote component information into local memory; and

issuing an imperative to the local addressing machine to initiate the remote operation.

7. The method of claim 6 wherein the addressing machine performs the steps of:

receiving an imperative from the local processing machine;

retrieving remote component information from the local memory, wherein the remote component information comprises a local geographic address, a remote geographic address, and a remote local memory address;

generating a meta-address responsive to the retrieved remote component information;

generating a data packet responsive to the generated meta-address; and

sending the data packet to the interconnect unit.

8. A method for addressing memory in a parallel computing environment in which local processing units are coupled to local memory, local addressing machines, and an interconnect unit, the addressing machine performing the steps of:

receiving a data packet;

decoding the data packet into a geographic address and a local address;

comparing the geographic address to an associated geographic address; and

responsive to the geographic address matching the associated geographic address, transmitting the data packet to the local processor.

9. The method of claim 8 wherein the step of transmitting the data packet to the local processor further comprises the step of storing the data packet in a queue for processing by the local processor.

10. The method of claim 8 further comprising the steps of:

receiving data from the local processor;

retrieving remote operation data from the local memory responsive to the received data;

generating a meta-address from the retrieved data;

generating a data packet responsive to the generated meta-address; and

transmitting the data packet to the interconnect unit.

11. The method of claim 10 wherein retrieving remote operation data comprises retrieving a remote geographic address and a remote local memory address.

12. The method of claim 11 further comprising retrieving a source geographic address from local memory.

13. The method of claim 12 in which architecture description memory is coupled to each processor and stores a geographic address for the local processor to which it is coupled, further comprising retrieving a source geographic address from architecture description memory.

14. A method for processing instructions in a parallel processor architecture having local processing machines coupled to local addressing machines and local memory, and the addressing machines are identified by unique geographic identifications and are interconnected through an interconnection unit, comprising the steps of:

receiving an imperative from the local processing machine;

retrieving remote component information from the local memory, wherein the remote component information comprises a local geographic address, a remote geographic address, and a remote local memory address;

generating a meta-address responsive to the retrieved remote component information;

generating a data packet responsive to the generated meta-address; and

sending the data packet to the interconnect unit.

15. A method for addressing memory in a parallel computing environment in which local processing units are coupled to local memory, local addressing machines, and an interconnect unit, the addressing machine performing the steps of:

receiving data from the local processor;

retrieving remote operation data from the local memory responsive to the received data;

generating a meta-address from the retrieved data;

generating a data packet responsive to the generated meta-address; and

transmitting the data packet to the interconnect unit.